REMARKS/ARGUMENTS

1. Claims 2, 10 and 19 have been rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter.

   With respect to Claim 2, Applicant has amended the claim to provide antecedent basis for "the type of transfer".

   With respect to Claims 10 and 19, Applicant has amended the claims to provide antecedent basis for "the length".

   Applicant submits that Claims 2, 10 and 19 now provide antecedent basis and respectfully requests that the rejection of Claims 2, 10 and 19 under 35 USC 112, second paragraph, be withdrawn.

2. Claims 1 - 19 have been rejected under 35 USC 102(b) as being anticipated by Pekkala (US 2002/0172195). Applicant notes that a rejection under 35 USC 102(b) requires that the reference particularly teach the claimed invention.

   Here, Pekkala does teach a point-to-point link as the Office Action notes. However, Pekkala introduces the concept of a transaction switch (302 in Fig. 3). In the claimed invention, each point-to-point link interfaces to a bus emulator. A bus emulator is entirely distinct from Pekkala's transaction switch. Accordingly, Applicant submits that the rejection of Claims 1 – 19 under 35 USC 102(b) must be withdrawn.

   According to Applicant's teachings, the each local bus is converted to a point-to-point link. Each point-to-point link is communicatively coupled to the bus

emulator. The bus emulator, as described by Applicant on Page 9, Lines 9 – 12) includes an internal bus with which all point-to-point interfaces are communicatively coupled to. As such, this internal bus really is a bus where only one transfer can be accommodated at any given time.

In Pekkala, the transaction switch includes, according to Fig. 4, shared memory 404 and multiplexers 402,406. Transfer of data through the transaction switch is accomplished under control of control logic 408 also included in the transaction switch. The transaction switch provides multiple data paths that can be used concurrently to pass transactions from port to port. In other words, the transaction switch is more akin to a network switch than it is to a computer bus. The problem with this is that a network switch necessarily introduces latency and a non-deterministic manner of operation when one bus master needs to communicate with a memory mapped device on a different bus. As Applicant claims, the bus emulator is a bus that can have contention as different point-to-point interfaces vie for access to the bus. This results in a more deterministic access profile and prevents out-of-sequence access across the bus.

3. Based on the foregoing, Applicant considers the present invention to be distinguished from the art of record. Accordingly, Applicant respectfully solicits the Examiner's withdrawal of the rejections raised in the above referenced Office Action, such that a Notice of Allowance is forwarded to Applicant, and the present application is therefore allowed to issue as a United States patent.

Respectfully Submitted,

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